AMENDMENTS TO THE CLAIMS:

This listing of claims will replace all prior versions, and listings, of claims in the application:

LISTING OF CLAIMS:

1-9. (canceled)

10. (currently amended) A reconfigurable architecture for a computer device having at least one individually configurable and/or reconfigurable sequential circuit which

- has a first stage with inputs and is formed from a plurality of parallel-connected memory elements which can be addressed via input lines, each memory element being able to be supplied with a subset of [[the]] input variables attached to an associated, ascertained implicant,
- has a second stage, connected downstream of the first stage, with memory elements which can be addressed by [[the]] identifiers of the individual implicants,

and

- has a third stage, connected downstream of the second stage, with outputs and with means for disjunctive logic combination of [[the]] output values from the individual implicants from the memory elements in the second stage,

where output variables from at least some of the outputs at a time t_{n-1} form the input variables on associated inputs of the sequential circuit at a time t_n and where means are provided for

clock-controlled storage of the output variables from the sequential circuit between the times t_{n-1} and t_n.

11. (previously presented) The architecture as claimed in claim 10, characterized in that the storage means are register memory elements.

12. (previously presented) The architecture as claimed in claim 10, characterized by implicants ascertained using minimization methods.

13. (previously presented) The architecture as claimed in claim 11, characterized by implicants ascertained using minimization methods.

14. (previously presented) The architecture as claimed in claim 10, characterized in that the first stage is logically combined with the second stage by means of at least one crossbar switch.

15. (previously presented) The architecture as claimed in claim 10, characterized by CAMs and/or RAMs as memory elements.

16. (previously presented) The architecture as claimed in claim 10, characterized by implementation of at least one GCA.

17. (previously presented) The architecture as claimed in claim 10, characterized by magnetoresistive memory elements, particularly of the TMR type.